What is claimed is:

1. A clock recovery device comprising:

a sample component that obtains center and edge samples of a serial data stream;

a number of voting components that identify early and late operation for a set of consecutive bit times of the serial data stream from the obtained center and edge samples; and

an analyzer that generates an average operation for the set of consecutive bit times from identified operations of the number of voting components.

2. The device of claim 1, further comprising a data clock and a transition clock, wherein the sample component employs the data clock to obtain center samples and the transition clock to obtain edge samples.

3. The device of claim 2, wherein the center samples are obtained on a rising edge of the data clock and the edge samples are obtained on a rising edge of the transition clock.

4. The device of claim 2, wherein the analyzer component adjusts operation of the data clock and the transition clock according to the average operation of the set of consecutive bit times.

5. The device of claim 1, wherein the set of consecutive bit times comprises 8 bits.

6. The device of claim 1, wherein the set of consecutive bit times comprises 16 bits.

7. The device of claim 1, wherein the number of voting components respectively obtain a previous center sample, a current edge sample, and a current center sample from the sample component for one of the consecutive bit times and identify early and late operation for the one bit time according to the previous center sample, the current edge sample, and the current center sample.

8. A voting component comprising:

a current center sample input node that receives a current center sample;

a current edge sample input node that receives a current edge sample;

a previous center sample input node that receives a previous center sample;

an early output node that selectively draws a reference current according to the current center sample, the current edge sample, and the previous center sample;

a late output node that selectively draws the reference current according to the current center sample, the current edge sample, and the previous center sample; and

circuitry for selectively controlling the early output node and the late output node.

9. The voting component of claim 8, wherein the first reference current and the second reference current are about equal.

10. The voting component of claim 8, further comprising:

a complement center sample node that receives a logical complement of the current center sample;

a complement edge sample node that receives a logical complement of the current edge sample; and

a complement previous center sample node that receives a logical compliment of the previous center sample.

11. The voting component of claim 10, wherein the circuitry comprises:

a first transistor having a drain connected to the late output node and a gate connected to the complement previous center sample node;

a second transistor having a drain connected to a source of the first transistor and a gate connected to the current edge sample input node;

a third transistor having a drain connected the early output node and a gate connected to VDD;

a fourth transistor having a drain connected to a source of the third transistor and a gate connected to the complement edge sample node;

a fifth transistor having a drain connected to a source of the second transistor and a source of the fourth transistor and a gate connected to the current center sample input node;

a sixth transistor having a drain connected to the late output node and a gate connected to the previous center sample input node;

a seventh transistor having a drain connected to a source of the sixth transistor and a gate connected to the complement edge sample node;

an eighth transistor having a drain connected to the early output node and a gate connected to VDD;

a ninth transistor having a drain connected to a source of the eighth transistor and a gate connected to the current edge sample input node;

a tenth transistor having a drain connected to a source of the seventh transistor and a source of the ninth transistor and a gate connected to the complement center sample node; and

a reference current circuit connected to a source of the fifth transistor and a source of the tenth transistor that draws the reference current from the early

output node or the late output node according to the current center sample, the current edge sample, and the previous center sample.

12. The voting component of claim 10, wherein the circuitry comprises an inverter generates the logical complement of the current center sample from the current center sample.

13. The voting component of claim 8, wherein the early output node selectively draws a reference current based on a logical expression of the current center sample XORed with the current edge sample.

14. A clock recovery device comprising:

a sample component that obtains center and edge samples of a serial data stream;

a number of voting components that identify early and late operation for a set of consecutive bit times of the serial data stream from the obtained center and edge samples and selectively draw a reference current at early and late output nodes according to the identified operation; and

an analyzer that measures and compares current drawn by the number of voting components at the early and late output nodes and indicates an average operation based upon the comparison.

15. The device of claim 14, wherein the analyzer comprises:

a composite early node connected to the early output nodes of the number of voting components;

a composite late node connected to the late output nodes of the number of voting components;

a first resistor having a first terminal connected to VDD and a second terminal connected to the composite early node;

a second resistor having a first terminal connected to VDD and a second terminal connected to the composite late node;

a third resistor having a first terminal connected to the composite early node;

a composite early plus node connected to a second terminal of the third resistor;

a fourth resistor having a first terminal connected to the composite late node;

a composite late plus node connected to a second terminal of the fourth resistor;

a first reference current circuit connected to the composite early plus node that draws a half of the reference current;

a second reference current circuit connected to the composite late plus node that draws a half of the reference current;

a first comparator that compares a voltage of the composite early node to a voltage of the composite late plus node and generates a early output on the voltage of the composite early node being less than the voltage of the composite late plus node; and

a second comparator that compares a voltage of the composite plus early node to a voltage of the composite late node and generates a late output on the voltage of the composite late node being less than the voltage of the composite early plus node, wherein the early output and the late output indicate the average operation of the set of consecutive bit times.

16. The device of claim 15, wherein the first resistor, the second resistor, the third resistor, and the fourth resistor have substantially similar resistance values.

17. The device of claim 16, wherein the voting components respectively comprise:

a current center sample input node that receives a current center sample;

a current edge sample input node that receives a current edge sample;

a previous center sample input node that receives a previous center sample;

an early output node that selectively draws a reference current according to the current center sample, the current edge sample, and the previous center sample;

a late output node that selectively draws the reference current according to the current center sample, the current edge sample, and the previous center sample;

a complement center sample node that receives a logical complement of the current center sample;

a complement edge sample node that receives a logical complement of the current edge sample;

a complement previous center sample node that receives a logical compliment of the previous center sample

a first transistor having a drain connected to the early output node and a gate connected to the complement previous center sample node;

a second transistor having a drain connected to a source of the first transistor and a gate connected to the current edge sample input node;

a third transistor having a drain connected the late output node and a gate connected to VDD;

a fourth transistor having a drain connected to a source of the third transistor and a gate connected to the complement edge sample node;

a fifth transistor having a drain connected to a source of the second transistor and a source of the fourth transistor and a gate connected to the current center sample input node;

a sixth transistor having a drain connected to the early output node and a gate connected to the previous center sample input node;

a seventh transistor having a drain connected to a source of the sixth transistor and a gate connected to the complement edge sample node;

an eighth transistor having a drain connected to the late output node and a gate connected to VDD;

a ninth transistor having a drain connected to a source of the eighth transistor and a gate connected to the current edge sample input node;

a tenth transistor having a drain connected to a source of the seventh transistor and a source of the ninth transistor and a gate connected to the complement center sample node; and

a third reference current circuit connected to a source of the fifth transistor and a source of the tenth transistor that draws the reference current from the early output node and the late output node according to the current center sample, the current edge sample, and the previous center sample.

18. A method of detecting early/late operation of clocks comprising:

obtaining center and edge samples of a received serial data stream for a set of consecutive bit times according to data and transition clocks;

analyzing the set of consecutive bit times to identify late operation(s) of the clocks within the respective consecutive bit times according to the obtained center and edge samples;

analyzing the set of consecutive bit times to identify early operation(s) of the clocks within the respective consecutive bit times according to the obtained center and edge samples; and

comparing the identified late operation(s) with the identified early operation(s) to determine average clock operation over the set of consecutive bit times.

19. The method of claim 18, further comprising adjusting data and transition clocks according to the determined average clock operation over the set of consecutive bit times.

20. The method of claim 18, wherein obtaining center samples comprises sampling the received serial data stream on rising edges of a data clock.

21. The method of claim 20, wherein obtaining edge samples comprises sampling the received serial data stream on rising edges of a transition clock.

22. The method of claim 18, wherein analyzing the set of consecutive bit times to identify late operation(s) comprises identifying a transition between a current edge sample and a previous center sample for each bit time.

23. The method of claim 18, wherein analyzing the set of consecutive bit times to identify early operation(s) comprises identifying a transition between a current edge sample and a current center sample for each bit time.